S/N 09/256,643



IN THE UNITED STAT AND TRADEMARK OFFICE

Applicant:

Leonard Forbes et al.

Serial No.:

09/256,643

Filed: Title:

February 23, 1999

TRANSISTOR WITH

Examiner:

Group Art Unit: 2822

Docket: 303.324US2

ARIABLE ELECTRON AFFINITY GATE AND

METHODS OF FABRICA TO NAND USE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. §1.97(b)(3), it is believed that no fee or certificate is required with this Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication RECEIVED

AUG 3 0 1999

Respectfully submitted,

TECHNOLOGY CENTER 2800

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6973

Robert E Reg. No. 35,271

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on August 2 1999.

GAU 2822



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Leonard Forbes et al.

Title:

TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND

USE

Docket No.:

303.324US2 **HE**(

RECEIVED

Serial No.: 09/256,643

Filed:

February 23, 1999

Due Date: September 23, 1999 Group Art Unit: 2822

Examiner:

Assistant Commissioner for Patents

TECHNOLOGY CENTER 2800

AUG 3 0 1999

Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.

X A Supplemental Information Disclosure Statement (1 pgs.), Form 1449 (1 pgs.), and copies of 1 cited references.

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described above, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 23 day of August, 1999.

SCHWEGMAN; LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

Atty: Robert E. Mates

Reg. No. 35,271

Customer Number 21186

(GENERAL)